**VLSI Code Using Vivado**

* **Code:**

module AND(

input a,b,

output y

);

assign y = a&b;

endmodule

* **Test bench:**

module AND1( );

wire y;

reg a,b;

AND dut(a,b,y);

initial

begin

a =0;

b=0;

#10 a=1;b=1;

end

endmodule

* **Output:**



